REMARKS

Claims 17, 18 and 22-24 are pending and under consideration. Claim 17 has been amended. Claims 22-24 are newly added. No new matter is believed to have been added.

Reconsideration is respectfully requested.

I. Rejections under 35 U.S.C. §102(b)

Claims 17 and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kusano (JP 10-302277 ('277)). This rejection is respectfully traversed.

The reference of record, '277, discloses an optical device with *a phase comparator with automatically variable frequency waveform*, which can change frequency characteristics in accordance with an **external input from** the **PLL circuit 7**. (See electronic translation page 11 paragraphs 0064 and 0066 and FIGs. 13 and 14) (Emphasis added). The '277 reference discloses that D flip flops 151 and 153 together with the NOR gates 159 and 160 are equivalent to the conventional phase comparator 26 in FIG. 2. D flip-flops 161 and 162 are adjustable monostable multivibrators which adjust a time constant based on an external input voltage level.

The Action still equates element 127 and elements 161 and 164 from drawings 13 and 14, respectively, as disclosing a Phase lock loop circuit (PLL). Applicant respectfully disagrees because nothing in the machine translation supports this interpretation. The Examiner's contention that element 127 corresponds to the claimed phase lock loop is completely unsubstantiated and contrary to the '277 disclosure's own teachings. The '277 reference provides in the machine translation, both in the drawings and the text, that element 7 is a phase lock loop (PLL) circuit, for example at page 11, paragraphs 0064 and 0066, among other citations. For example, "the signal PLCK of the PLL circuit 7 (refer to drawing 1) pass to the FV converter 163," clearly indicates that element 127 is not the PLL circuit (i.e., element 7 of drawing 1). Note that the reference refers to element 7 as a "PLL circuit," but element 127 is never referred to as a "PLL circuit." Absent some explicit evidence that has yet to be provided by the Examiner, there is no reason to disregard the direct teachings and disclosure of the '277 reference that element 7, not element 127, is the Phase Lock Loop (PLL) circuit.

In contrast, claim 17 of the present invention recites that the phase lock loop (PLL) circuit *receives* a first clock signal having a higher frequency than the matrixed signals and each matrixed signal, not *produces* a first clock signal (PLCK) as the reference discloses. As described above, element 127 makes up the *phase comparator with automatically variable*

frequency waveform. The PLL circuit is element 7 as shown in drawing 1.

The Action equates the PLCK signal with the "first clock signal" recited in claim 17. However, as shown in FIG. 1 of the cited '277 reference the PLL circuit 7 is not located in element 127. Rather, the PLL circuit 7 (i.e., the phase lock loop) provides a clock signal PLCK to element 127 in drawing 13. The PLL circuit 7 does not provide a PLCK to any other PLL circuit or the disclosure would indicate such a relationship. Thus, there is no basis for interpreting the disclosure in a manner contrary to its own teachings.

Further, the '277 reference does not disclose that the PLL circuit 7 receives any of the matrixed signals as recited in claim 17. Rather, in the '277 reference, the matrixed signals (i.e., a1 and b1 in drawing 13) are never processed in the PLL circuit 7 and are processed separately from the circuit 7 as shown in the drawings 1, 13 and 14.

Further support that element 127 is not a PLL circuit is provided in the '277 reference description because the outputs are not clock signals synchronized to the matrixed signals, contrary to the assertion in the Action. Signals a5 and b5 in FIG. 12 clearly show that one signal a5 is tracking the pit marks and the other signal b5 is a flat line. Thus, a5 and b5 are not "second and third **clock signals** synchronized with the respective matrixed signals" as recited in independent claim 17. Also, as seen in FIG. 12 the tracking error signal based on a5 and b5 is based on the pits detected on the disc as shown by signals a2 and b2. A flat line is not a clock signal and is not synchronized with any other signal.

In contrast, amended claim 17 recites "a phase lock loop circuit receiving a first clock signal having a higher frequency than the matrixed signals and each matrixed signal, the phase lock loop circuit outputting second and third clock signals synchronized with the respective matrixed signals and having the same frequency as the first clock signal; and a phase detector which compares a phase of the second synchronized clock signal with a phase of the third synchronized clock signal to generate the tracking error signal, wherein the tracking error signal is independent of a length of pits and/or marks on the optical disk recording track."

In view of the foregoing, Applicant respectfully submits that independent claim 17 patentably defines the present invention over the citations of record. Further, the dependent claim 18 should also be allowable for the same reasons as its respective base claim and further due to the additional features recited.

II. New claims

Claims 22-24 are newly added. Claim 22 is the independent claim. The references of record do not teach or suggest that the phase locked loops generate clock signals synchronized with each of the outputs of the plurality of binarizers. As discussed above, the '277 reference discloses that the outputs to element 127 (i.e., a5 and b5) are **not clock signals**. One of the signals output from element 127 is a flat line, which is not a clock signal and is not usable as such. This only further establishes that element 127 is not a phase lock loop (PLL). The Examiner is ignoring the fact that the cited reference describes element 7 as a phase locked loop and labels it PLL. The clock output from element 7 is further labeled in line with this identification as PLCK. However, even assuming for the sake of argument only that element 127 is a phase lock loop, the outputs a5 and b5 are not synchronized with each of the outputs of the plurality of binarizers as recited in new claim 22. In fact, output b5 is a flat line which is unsynchronized to anything. It is respectfully submitted that in view of the above, that independent claim 22 patentably distinguishes the present invention over the citations of record.

Further, the dependent claims 23-24 should also be allowable for the same reasons as their respective base claim and further due to the additional features recited.

III. Conclusion

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Applicants submit that this Amendment After Final Rejection clearly places the subject application in condition for allowance. This Amendment was not earlier presented, because Applicants believed that the prior Amendment placed the subject application in condition for allowance. Accordingly, entry of the instant Amendment as an earnest attempt to advance prosecution and reduce the number of issues is requested under 37 C.F.R. § 1.116.

Applicants believe that the present Amendment is responsive to each of the points raised by the Examiner in the Official Action. However, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to such matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 503333.

Respectfully submitted,

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